05SCS11/05SCE11

USN | | | | | | | | | | |

NEW SCHEME

First Semester M.Tech. Degree Examination, June 2007

Computer Architecture

Time: 3 hrs.] [Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. Explain the Flynn's classification of Computer Architecture. **(06 Marks)**

b. Consider an execution of a program of 20,000 instructions by a linear pipeline processor with a clock rate of 100 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out of sequence executions are ignored.

i) Calculate the speedup factor in using this pipeline to execute the speed up factor in using this pipeline to execute the program as compared with the use of an equivalent non-pipe lined processor with an equal amount of flow-through delay.

ii) Find the efficiency and throughput of this pipelined processor. **(06 Marks)**

c. With neat block diagram explain any two shared memory multiprocessor models. **(08 Marks)**

2 a. Distinguish VLIW and Super scalar ILP processors. **(06 Marks)**

b. What is Data dependency? Explain the different types of data dependencies that could arise in straight-line code execution in ILP processors. **(07 Marks)**

c. With block diagram, explain the principle of BTAC and BTIC schemes of accessing the branch target path. **(07 Marks)**

3 a. A certain dynamic pipeline with the three segments S_1, S_2 and S_3 is characterized by the following reservation table:

	t_0	t_1	t_2	t_3	t_4	t_5
S_1	X				X	
S_2			X			
S_3		X		X		X

Fig.3(a)

i) Determine the latencies in the forbidden list F and collision vector C.

ii) Draw the state diagram for this pipeline.

iii) List all simple and greedy cycles.

iv) Determine MAL associated with the shortest greedy cycle.

v) Determine the lower bound on the MAL for this pipeline. **(10 Marks)**

b. Draw the layout of the pipeline of the power PC 620. Explain the main features of its micro architecture. **(10 Marks)**

4 a. With an example, explain the implementation of super scalar CISC Processors using a super scalar RISC core. **(10 Marks)**

b. With relevant diagram, explain any two interconnection networks that can implement all communication patterns based on program demands. **(10 Marks)**

Contd...2

5 a. What is meant by granularity of an SIMD system? With necessary diagram, explain the features of an example fine-grained SIMD architecture. **(10 Marks)**

b. What is cache coherence? Explain any bus snooping protocol to maintain cache-coherence. **(10 Marks)**

6 a. Differentiate the Data flow architecture from control flow (von neumann) architecture. **(06 Marks)**

b. Draw the Data flow graph to obtain an approximation of cos(x) by computation of the following series.

$$\cos(x) \simeq 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!}$$ **(06 Marks)**

c. Explain the method of obtaining synchronization among P – processors in a bus based multiprocessor systems. **(08 Marks)**

7 a. What is vector processing? Explain the cray C90 system architecture. **(10 Marks)**

b. With an example, explain the principle of operation of systolic architecture. **(10 Marks)**

8 Write short notes on :

a. Reservation stations. **(07 Marks)**

b. CSA pipe for integer multiplication. **(08 Marks)**

c. Hyper cube routing function. **(07 Marks)**

*****